IN THE CLAIMS

Please cancel claims 3-5, 9, 15, and 19-30.

Please add new claims 31-45.

The pending claims are as follows:

1. (Currently Amended) An interposer to couple a die to a substrate and comprising:

a plurality of power and ground vias in a core region of the interposer;

an embedded [[a]] capacitor having first and second terminals;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias; and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die through controlled collapse chip connect solder bumps.

~~a first plurality of lands on a first surface thereof, including a first land coupled to the first terminal and a second land coupled to the second terminal; and~~

~~a second plurality of lands on a second surface thereof, including a third land coupled to the first terminal and a fourth land coupled to the second terminal.~~

2. (Currently Amended) The interposer recited in claim 1 wherein the second plurality of power lands and the second plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the substrate ~~wherein the first and second lands are positioned to be coupled to corresponding power supply nodes of the die, and wherein the third and fourth nodes are positioned to be coupled to corresponding power supply nodes of the substrate~~.

3-5. (Canceled)

6. (Original) The interposer recited in claim 1 wherein the capacitor comprises at least one high permittivity layer.

7. (Original) The interposer recited in claim 1 wherein the capacitor comprises a plurality of high permittivity layers.

8. (Currently Amended) The interposer recited in claim 7 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals [[lands]], respectively.

9. (Canceled)

10. (Original) The interposer recited in claim 1 wherein the first plurality of lands comprises a fifth land positioned to be coupled to a corresponding signal node of the die, and wherein the second plurality of lands comprises a sixth land positioned to be coupled to a corresponding signal node of the substrate.

11. (Original) The interposer recited in claim 10 wherein the fifth and sixth lands are coupled by a conductive path that comprises at least one via.

12. (Currently Amended) An electronic assembly comprising:

a die comprising a first plurality of power nodes and a first plurality of ground nodes;

a substrate comprising a second plurality of power nodes and a second plurality of ground nodes; and

~~a die comprising first and second power supply nodes;~~

~~a substrate having third and fourth power supply nodes; and~~

an interposer coupling the die to the substrate and including

a plurality of power and ground vias in a core region of the interposer;

an embedded capacitor having a first terminal and a second terminal;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias; and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are coupled to the respective first plurality of power nodes and first plurality of ground nodes of the die; and

wherein the second plurality of power lands and the second plurality of ground lands are coupled to the respective second plurality of power nodes and second plurality of ground nodes of the substrate.

~~an interposer coupling the die to the substrate and comprising:~~

~~a capacitor having first and second terminals;~~

~~a first plurality of lands on a first surface thereof, including a first land coupled to the first power supply node and the first terminal, and further including a second land coupled to the second power supply node and the second terminal; and~~

~~a second plurality of lands on a second surface thereof, including a third land coupled to the third power supply node and the first terminal, and further including a fourth land coupled to the fourth power supply node and the second terminal.~~

13. (Original) The electronic assembly recited in claim 12 wherein the capacitor comprises a plurality of high permittivity layers.

14. (Currently Amended) The electronic assembly recited in claim 13 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals ~~lands~~, respectively.

15. (Canceled)

16. (Currently Amended) An electronic system comprising an electronic assembly comprising:

a die comprising a first plurality of power nodes and a first plurality of ground nodes;

a substrate comprising a second plurality of power nodes and a second plurality of ground nodes; and

~~a die comprising first and second power supply nodes;~~

~~a substrate having third and fourth power supply nodes; and~~

an interposer coupling the die to the substrate and including

a plurality of power and ground vias in a core region of the interposer;

an embedded capacitor having a first terminal and a second terminal;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias; and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are coupled to the respective first plurality of power nodes and first plurality of ground nodes of the die; and

wherein the second plurality of power lands and the second plurality of ground lands are coupled to the respective second plurality of power nodes and second plurality of ground nodes of the substrate.

~~an interposer coupling the die to the substrate and comprising:~~

~~a capacitor having first and second terminals;~~

~~a first plurality of lands on a first surface thereof, including a first land coupled to the first power supply node and the first terminal, and further including a second land coupled to the second power supply node and the second terminal; and~~

~~a second plurality of lands on a second surface thereof, including a third land coupled to the third power supply node and the first terminal, and further including a fourth land coupled to the fourth power supply node and the second terminal.~~

17. (Original) The electronic system recited in claim 16 wherein the capacitor comprises a plurality of high permittivity layers.

18. (Currently Amended) The electronic system recited in claim 17 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals ~~lands~~, respectively.

19-30. (Canceled)

31. (New) The interposer recited in claim 1 further comprising:

a plurality of signal vias in a peripheral region of the interposer;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

32. (New) The interposer recited in claim 1, wherein the interposer comprises a multilayer ceramic structure.

33. (New) The interposer recited in claim 1, wherein at least one of the power vias does not go entirely through the interposer.

34. (New) The interposer recited in claim 1, wherein at least one of the ground vias does not go entirely through the interposer.

35. (New) The interposer recited in claim 1, wherein the plurality of power and ground vias is a relatively large number.

36. (New) An interposer to couple a die to a substrate and comprising:

a plurality of power and ground vias in a core region of the interposer;

an embedded capacitor having a first terminal and a second terminal;

a first surface including a first plurality of power lands coupled to the first terminal through the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through the plurality of ground vias; and

a second surface including a second plurality of power lands coupled to the first terminal through the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die through controlled collapse chip connect solder bumps.

37. (New) The interposer recited in claim 36 wherein the second plurality of power lands and the second plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the substrate.

38. (New) The interposer recited in claim 36 wherein the capacitor comprises at least one high permittivity layer.

39. (New) The interposer recited in claim 36 wherein the capacitor comprises a plurality of high permittivity layers.

40. (New) The interposer recited in claim 39 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals, respectively.

41. (New) The interposer recited in claim 36 further comprising:

a plurality of signal vias in a peripheral region of the interposer;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

42. (New) The interposer recited in claim 36, wherein the interposer comprises a multilayer ceramic structure.

43. (New) The interposer recited in claim 36, wherein at least one of the power vias does not go entirely through the interposer.

44. (New) The interposer recited in claim 36, wherein at least one of the ground vias does not go entirely through the interposer.

45. (New) The interposer recited in claim 36, wherein the plurality of power and ground vias is a relatively large number.